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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

**Complete if Known**

Application Number	
Filing Date	November 11, 2003
First Named Inventor	William J. Borland
Art Unit	3729
Examiner Name	D. N. KUYER
Attorney Docket Number	EL 0509 US NA

Sheet 1 of 2

**U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
DN		US- 6,317,023 B1	11-13-2001	FELTEN	
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**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				

Examiner Signature	<i>Ashtyn</i>	Date Considered	11/11/05
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Substitute for form 1449B/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Complete if Known</b>			
		Application Number			
		Filing Date	November 11, 2003		
		First Named Inventor	William J. Borland		
		Art Unit	3729		
		Examiner Name	Da NGUYEN		
Sheet	2	of	2	Attorney Docket Number	EL 0509 US NA

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
Da		FELTEN, J., FERGUSON, S., Embedded Ceramic Resistors and Capacitors in PWB - Process and Design, IPC Printed Circuits Expo, Long Beach, California, March 2002	<input type="checkbox"/>
Da		FELTEN, J., SNOGREN, R., AND ZHOU, J., Embedded Ceramic Resistors and Capacitors in PWB: Process and Performance, Fall IPC Meeting, Orlando, Florida, October 11, 2001	<input type="checkbox"/>
Da		BORLAND, W., FELTEN, J., Thick Film Ceramic Capacitors and Resistors inside Printed Circuit Boards, 34th International Symposium on Microelectronics (IMAPS), Baltimore, MD., October 9-11, 2001	<input type="checkbox"/>
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Examiner Signature	<i>Do Nguyen</i>	Date Considered	11/11/03
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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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**Complete If Known**

Application Number	10/718,044
Filing Date	November 20, 2003
First Named Inventor	William J. Borland
Art Unit	3729
Examiner Name	D. NGUYEN
Attorney Docket Number	EL0509 US NA

Sheet 2 of 3

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Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
mn		JOHN FELTEN AND SAUL FERGUSON, Embedded Ceramic Resistors and Capacitors for PWB, IP Printed Circuit Expo, San Diego, CA, April 2000.	<input type="checkbox"/>
gn		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IPC, San Diego, April 5, 2000.	<input type="checkbox"/>
bn		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IMAPS, Denver, April 29, 2000.	<input type="checkbox"/>
gn		JOHN J. FELTEN AND WILLIAM J. BORLAND, Embedded Ceramic Passives in PWB: Process Development, IPC Printed Circuit Expo, Anaheim, CA, April 2001.	<input type="checkbox"/>
mn		JOHN J. FELTEN AND WILLIAM J. BORLAND, Ceramic Resistors and Capacitors Embedded in PWB's, IPC Expo, April 3, 2001.	<input type="checkbox"/>
ON		WILLIAM BORLAND, Designing for Embedded Passives, Printed Circuit Design, August 2001.	<input type="checkbox"/>

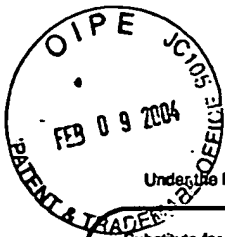
Examiner  
SignatureDate  
Considered

11/11/05

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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**Complete If Known**

Application Number	10/718,044
Filing Date	November 20, 2003
First Named Inventor	William J. Borland
Art Unit	3729
Examiner Name	D. NGUYEN
Attorney Docket Number	EL0509 US NA

Sheet 3 of 3

**NON PATENT LITERATURE DOCUMENTS**

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DN		DR. KIM FJELDSTED AND STACEY L. CHASE, Embedded Passives: Laser Trimmed Resistors, CircuitTree, Volume 70, March 2002.	<input type="checkbox"/>
DN		WILLIAM J. BORLAND AND SAUL FERGUSON, Embedded Passive Components in Printed Wiring Boards, a Technology Review, To be published in CircuitTree Magazine, 2001.	<input type="checkbox"/>
DN		JIMING ZHOU, JOHN D. MYERS AND JOHN J. FELTEN, Embedded Passives Technology for PCBs: Materials, Design, and Process, IMAPS 2002 Conference, Denver, CO, Sept. 4-6, 2002.	<input type="checkbox"/>
DN		JOHN J. FELTEN, Electronic Circuits World Convention, Paper number IPC31, Advanced Embedded Passives Technologies - Putting Ceramic Components into Organic PWBs.	<input type="checkbox"/>
DN		WILLIAM BORLAND, JOHN J. FELTEN, SAUL FERGUSON, ALTON B. JONES AND ANGELA A. LAWRENCE, Embedded Singulated Ceramic Passives in Printed Wiring Boards, IMAPS Advanced Technology Workshop on Passive Integration, Ogunquit, ME, June 19-21, 2002.	<input type="checkbox"/>
DN		RICHARD C. SNOGREN, Embedded Passives, a Review, IPC Designers Learning Symposium, October 3, 2002, Toronto ON, CN.	<input type="checkbox"/>

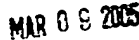
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SignatureDate  
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11/11/05

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*(Use as many sheets as necessary)*

Sheet	1	of	2
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**Complete if Known**

Application Number	10/718,044
Filing Date	November 20, 2003
First Named Inventor	William J. Borland E
Art Unit	2841-3729
Examiner Name	D. Nguyen
Attorney Docket Number	EL0509USNA

## U. S. PATENT DOCUMENTS

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## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. 1	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T 6
		Country Code 2-Number 4-Kind Code* (if known)				
BN		EP 1 265 466 A	12-11-2002	Dai Nippon Printing Co. Ltd.		
BN		EP 1 307 079 A	05-02-2003	Adtec Engineering Co., Ltd.		

Exam taker Signature	<i>Onshayuren</i>	Date Considered	11/11/05
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Substitute for form 1449B/PTO				<b>Complete If Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				Application Number	10/718044
				Filing Date	November 20, 2003
				First Named Inventor	William J. Borland Et. Al.
				Art Unit	2841 3729
				Examiner Name	D. NGUYEN
Sheet	2	of	2	Attorney Docket Number	EL0509USNA

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mv		Patent Abstracts of Japan, Vol. 1998, No. 06, 30 April 1998 (1998-04-30) & JP 10 051143 A (Oki Purintetsudo Circuit KK), 20 February 1998 (1998-02-20), Abstract	<input type="checkbox"/>
mv		Patent Abstracts of Japan, Vol. 2000, No. 02, 29 February 2000 (2000-02-29) & JP 11 330316 A (Nec Tohoku Ltd), 30 November 1999 (1999-11-30), Abstract	<input type="checkbox"/>
mv		Patent Abstracts of Japan, Vol. 2000, No. 22, 9 March 2001 (2001-03-09) & JP 2001 135941 A (Matsushita Electric Works Ltd.), 18 May 2001 (2001-05-18), Abstract	<input type="checkbox"/>
mv		Patent Abstracts of Japan, Vol. 2000, No. 16, 8 May 2001 (2001-05-08) & JP 2001 022099 A (Adtec Engineering Co. Ltd.), 26 January 2001 (2001-01-26), Abstract	<input type="checkbox"/>
			<input type="checkbox"/>
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Examiner Signature	<i>D. Nguyen</i>	Date Considered	11/11/03
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